IN THE CLAIMS

A complete list of claims is presented below with amendments marked up:

1-12. (Canceled).

13. (Previously Presented) An apparatus comprising:

a plurality of processors, wherein one of the plurality of processors is operable to cause remaining processors of the plurality of processors to pause execution of a plurality of threads before initiating a frequency calculation thread on the one of the plurality of processor to prevent interrupting the frequency calculation thread; and

a bus coupling the plurality of processors to each other.

14. (Original) The apparatus of 13, further comprising a performance monitor counter coupled to each of the plurality of processors to keep track of when the processor is active.

15. (Original) The apparatus of 14, the performance monitor counter to provide a count for determining the processor utilization.

16. (Original) The apparatus of claim 13, wherein the plurality of processors comprise a plurality of logical processors to execute threads simultaneously.

17. (Original) The apparatus of claim 13, wherein execution of the predetermined unit of code causes the remaining processors to pause.

18-27. (Canceled).

28. (Previously Presented) A method comprising:

preparing to initiate a frequency calculation thread on one processor of a plurality of processors in a data processing system, said preparing comprising

pausing execution of a plurality of threads on remaining processors of the plurality of processors to prevent interrupting the frequency calculation thread;

initiating the frequency calculation thread after pausing the execution of the plurality of threads; and

resuming the execution of the plurality of threads when execution of the frequency calculation thread has been completed.

29. (Previously Presented) The method of claim 28, wherein preparing to initiate the frequency calculation thread further comprises:

firing a wait synchronization event from the one processor of the plurality of processors to the remaining processors of the plurality of processors; and

waiting for acknowledgement from the remaining processors of the plurality of processors before initiating the frequency calculation thread.

30. (Previously Presented) The method of claim 28, wherein the plurality of processors comprise logical processors.

31. (Previously Presented) The method of claim 28, wherein the plurality of processors comprise physical processors.

32. (Previously Presented) A physical machine-accessible tangible medium that provides instructions that, if executed by a processor, will cause the processor to perform operations comprising:

preparing to initiate a frequency calculation thread on one processor of a plurality of processors in a data processing system, said preparing comprising

pausing execution of a plurality of threads on remaining processors of the plurality of processors to prevent interrupting the frequency calculation thread;

initiating the frequency calculation thread after pausing the execution of the plurality of threads; and

resuming the execution of the plurality of threads when execution of the frequency calculation thread has been completed.

33. (Previously Presented) The physical machine-accessible tangible medium of claim 32, wherein preparing to initiate the frequency calculation thread further comprises:

firing a wait synchronization event from the one processor of the plurality of processors to the remaining processors of the plurality of processors; and

waiting for acknowledgement from the remaining processors of the plurality of processors before initiating the frequency calculation thread.

34. (Previously Presented) The physical machine-accessible tangible medium of claim 32, wherein the plurality of processors comprise logical processors.

35. (Previously Presented) The physical machine-accessible tangible medium of claim 32, wherein the plurality of processors comprise physical processors.